

Appl. No. 10/711,410
Amdt. dated August 3, 2006
Reply to Office action of May 05, 2006

REMARKS/ARGUMENTS

Claim Rejections

Claims 1, 14, 22, and 43 are rejected under 35 U.S.C. 102(c) as being
5 anticipated by Wu et al. (U.S. Patent No. 6,760,397).

Response:

Claim 1

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Applicant asserts that claim 1 is not anticipated by Wu (U.S. Patent
No. 6,760,397) because the teachings of Wu cannot “synchronously reset at
least a part of the plurality of cells.” The Examiner states that the step of
synchronously resetting in claim 1 (i.e. step c) of the present invention is
15 performed by the signal PgLoad of Wu. However, the signal PgLoad
disclosed by Wu is used to synchronize the loading of a new divisor value
for each dividing stage of the divider, but not to reset the dividing
operation of each dividing stage. Specifically, the signal PgLoad is a
program-load signal for synchronously loading a new divisor value into
20 each of the dividing stages within a safe-load period (see col. 5, lines
31-43, and ref. 410 in Fig. 4). It can be appreciated by those skilled in the
art that to load a divisor value into a dividing unit will not “reset” the
dividing operation of the dividing unit. Therefore, the role of the signal
PgLoad is irrelevant to the reset signal stated in claim 1 of the present
25 invention.

The present invention discloses (Para. 41, lines 13-16), “Once the

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divisor value changes, the reset signal is employed to reset all cells 10 ...
so that each cell 10 refreshes its dividing operation after being reset."

Additionally, the present invention further describes (see Para. 71, lines
9-14, and Fig. 11) "As shown in the timing diagram 450, regardless of the
5 original operation mode of each cell 30, all cells 30 are synchronously
reset and stop dividing operations while the reset signal is enabled
during time 452 through time 454. During this period, the signal output
from the first output node (Fo) of each cell 30... becomes logic 0." It is
clearly described that each cell of the divider of the present invention stops
10 its dividing operation during the reset period determined by the reset signal.
Accordingly, the dividing outputs of all dividing cells are reset to the
initial logic level (i.e. logic 0 in the shown embodiment of the present
invention) when the reset signal is enabled.

15 In Wu's disclosure (see Fig. 4), however, the dividing outputs of all
dividing stages are not reset to the same logic level when the signal PgLoad
(i.e. any of the edges 401, 402, 403, and 404) is active. For example, in
Wu's preferred embodiment, the signal MinI with active edge 401 is used
as the signal PgLoad. As can be seen in Fig. 4 of Wu, when the signal
20 PgLoad is active (i.e. at the edge 401), the dividing output MinJ3 of the
last stage J-last, the dividing output MinJ2 of the stage J3, and the dividing
output MinJ1 of the stage J2 are at logic 1, but the dividing output MinH of
the stage I, the dividing output MinG of the stage H, and the dividing
output MinF of the stage G are at logic 0. Obviously, there is a significant
25 difference between "synchronously resetting dividing cells" and
"synchronously loading divisor values into dividing stages". It is again
proved that the signal PgLoad is not equivalent to the reset signal of the
present invention.

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For the reasons explained above, the applicant believes that the independent claim 1 is patentably distinct from Wu's teachings and kindly requests the Examiner to reconsider the rejection placed on claim 1 of the present application.

Claims 2-13

Claims 2- 13 are dependent on claim 1, and should be allowed if the independent claim 1 is found allowable.

Claim 14

In reference to claim 14, since the signal PgLoad of Wu is not equivalent to the reset signal stated in the claim 14 as explained above, the applicant believes that the independent claim 14 is also patentably distinct from Wu's teachings and kindly requests the Examiner to reconsider the rejection placed on claim 14 of the present application.

Claims 17-21

Claims 17-21 are dependent on claim 14, and should be allowed if the independent claim 14 is found allowable.

Claim 22

Claim 22 is cancelled.

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Claims 23-25

Claims 23, 24, and 25 are respectively rewritten in independent form including all of the limitations of the base claim 22. As stated in the section **Allowable Subject Matter**, claims 23-25 are objected to as being dependent upon rejected base claim 22, but would be allowable if rewritten in independent form including all of the limitations of the base claim 22. Applicant believes that amended claims 23-25 have been placed in condition for allowance.

Claims 26-31

Claim 26 is amended to be dependent on the rewritten claim 25. Amended claim 26 and claims 27-31 are now dependent on amended claim 25, and should be allowed since the amended claim 25 has been placed in condition for allowance.

Claim 43

Claim 43 is cancelled.

Claims 44-47

Claims 44, 45, 46, and 47 are respectively rewritten in independent form including all of the limitations of the base claim 43. As stated in the section **Allowable Subject Matter**, claims 44-47 are objected to as being dependent upon rejected base claim 43, but would be allowable if rewritten in independent form including all of the limitations of the base claim 43.

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Applicant believes that amended claims 44-47 have been placed in condition for allowance.

Claims 48-50

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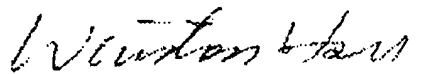
Claim 48 is amended to be dependent on the rewritten claim 47. Amended claim 48 and claims 49-50 are now dependent on amended claim 47, and should be allowed since the amended claim 47 has been placed in condition for allowance.

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Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

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